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Single Phase Full Bridge Inverter Formed by Floating Capacitors

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ABSTRACT:*In this paper, a new single-phase bridge inverter is described which can generate a more steps of voltage levels with reduced number of switches, gate driver circuits and diodes as compare to normal multilevel inverter. Another feature of this inverter is its ability to prodeuce the voltages from a single dc-link power supply which enables back-to-back operation of converter. The proposed method with more number of levels can improve power quality, lower switching losses and produce high quality voltage waveforms. Moreover at all load power factors the proposed method can be operated.The research of the model is done by means of computer simulation with the software MATLAB/SIMULINK. This topology has very low common mode voltage variation and dv/dt stress. Also this inverter is help full for rective powercompensation.*

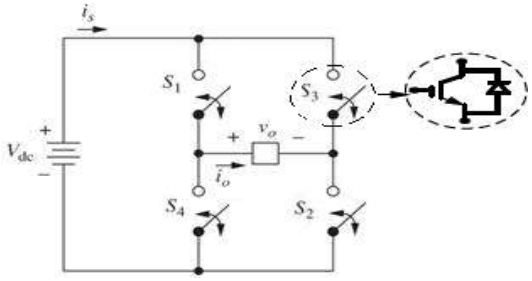
I. INTRODUCTION

Multilevel inverters are power electronic systems which produce a suitable AC output voltage waveform from many dc voltages as inputs [1]. Multilevel inverters have several features in comparison with the traditional two-level voltage inverters such as smaller output voltage level, better electromagnetic compatibility, lower harmonic components and lower switching losses [2], [3]. The conventional full bridge inverter output voltage or currents are of 0 or $\pm V_{dc}$ voltage. They are named as two-level inverter. In order to obtain a qualitative output voltage and current with reduced amount of ripple content, there is a necessity of high carrier frequency along with different pulse-width modulation (PWM) techniques. However In high- power applications these conventional square wave inverters have certain confines like conducting losses and device ratings. In modren years, Multilevel inverters have been utilized in medium and high power applications such as flexible AC transmission system (FACTS) [4], industrial motor drives [5], traction electric vehicle applications, drive systems [6], [7] and soon.

The output voltage waveform is almost a sinewave with minimum harmonic value, improving the performance of the drive presented in [8] and [9] as the number of voltage levels increases. The work described in [10] produces different voltage levels by switching the load current through capacitors. Here, by taking the redundant states for the same pole voltage, the direction of load current through the capacitor can be changed. In this paper, a novel structure for single phase full bridge inverter is presented which can produce more number of levels with minimum requirement of IGBTs, gate firing circuits and diodes.

II. THE STRUCTURE OF CONVENTIONAL SINGLE PHASEINVERTER

The structure of conventional square wave inverter is as follows like figure 1. In this structure, each switch consists of an IGBT and one diode (or anti-parallel diode). The output wave form of conventional system is shown in Figure 2.



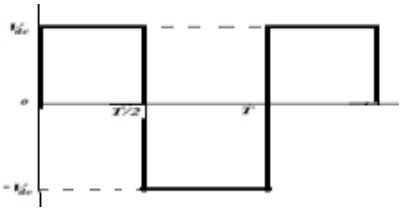


Figure 1. The arrangement of conventional inveter
Figure 2. Output wave form of Conventional system

By closing and opening the switches in an appropriate sequence we can get an ac output waveform is synthesized from a dc input. There are four different modes depending on which switches are closed. The equivalent circuits of all four modes are shown in Figure 3. The output current depends on load like R or RL. Mode 1: During this interval the switches S_1 and S_3 are closed. The output load voltage is zero i.e. load is shortcircuited.

$V_o = 0$ (1)

Mode 2: During this interval the switches S_1 and S_2 are closed. The output load voltage is equals to the input voltage (V_{dc}) i.e. load is connected across source directly. And the load current flows through V_{dc} - S_1- Load - S_2 and V_{dc}.

$V_o = V_{dc}$ (2)

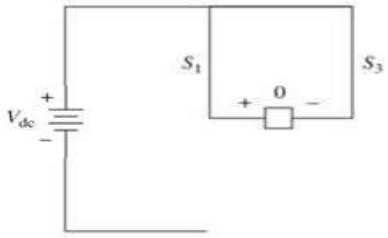


Figure 3(a).Mode1

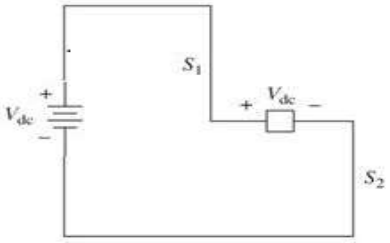


Figure 3(b). Mode2

In a similar manner the output voltage will have a negative of input voltage state and zero voltage state. $V_o = -V_{dc}$ (3)

And this cycle will repeats continuously.

The rms output voltage is,

$$V_o = \left(\frac{2}{T} \int_0^{T/2} Vdc^2 dt \right)^{1/2}$$

$$= V_{dc} \quad (4)$$

The Table 1 Shows the different swiching states of conventional full bridge inverter. Switches S1 and S4 or (S2 and S3) should not be turned on simultaneously. Otherwise, a dead zone interval takes place across the dc source.

Table 1. Switch states of Square wave inverter

Mode	On Position	Vo
1	S1 & S3	0
2	S1 & S2	+ Vdc
3	S2 & S4	0
4	S3 & S4	- Vdc

III. PROPOSEDINVERTER

The proposed structure of full bridge inverter is shown in Figure 4. In this structure, each switch contains of an IGBT and one diode (or anti-parallel diode) also one capacitor and one small resistor are connected across each switch. The proposed inverter gives a qualitative output voltage and current with reduced amount of ripple content. Also this inverter is help full in reactive power compensation.

By increasing the no of levels in this inverter, the power rating of inverter can be increased without requirement of high ratings devices. The unique structures of this proposed inverter allow reaching high voltage with minimum harmonic content without the usage of transformers or cascade connected switching devices. As the number of output levels increases, the output voltage harmonic content decreases significantly. The outputvoltagewave form of proposed system is as follows like Figure 5.

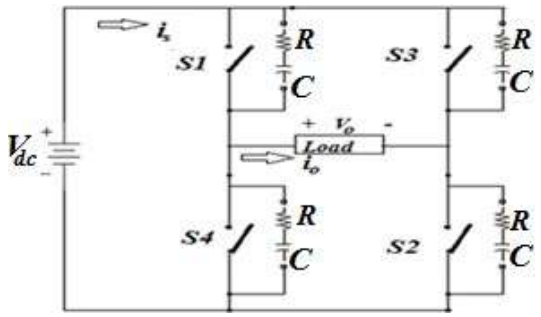


Figure 4. The Arrangement ofproposed inverter

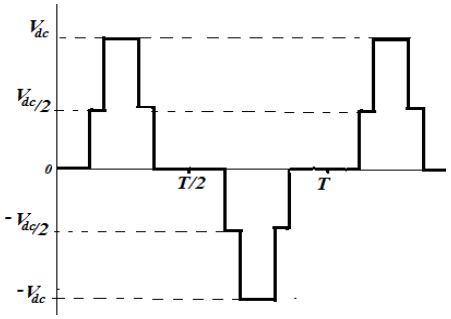


Figure 5. Output wave form of Conventional system

There are also eight different modes depending on which switches are closed. Theequivalentcircuits of all eight modes are follows like in Figure 6. The output current depends on load like R or RL. Mode 1: During this period the switches S_1 and S_3 are closed. The output load voltage is zero i.e. load is short circuited.

$V_o = 0$ (5)

Mode 2: During this period the switch S_1 is closed. The output load voltage is equals to the difference of input voltage (V_{dc}) and capacitor voltage (V_c). And the load current flows through V_{dc} - S_1- Load – capacitor and V_{dc}.

$V_o = V_{dc} - V_c = V_{dc}/2$ (6)

Here consider the voltage across the resistor is negligibleand$V_c \approx V_{dc}/2$.

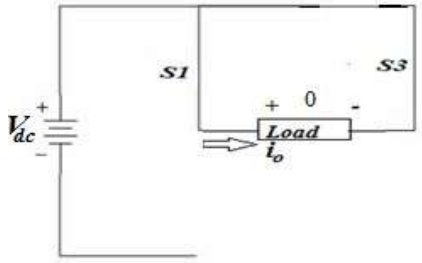


Figure 6(a).Mode1

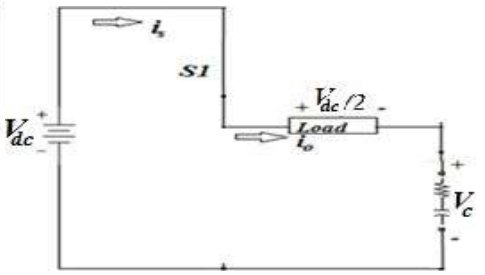


Figure 6(b). Mode2

Mode 3: During this period the switches S_1 and S_2 are closed. The output load voltage is equals to the input voltage (V_{dc}) i.e. load is connected across source directly. And the load current flows through V_{dc} - S_1- Load - S_2 and V_{dc}.

$V_o = V_{dc}$ (7)

Mode 4: Mode 2 and period4 are same only the switching sequence is different. During this period the switch S_2 is closed. The output load voltage is equals to the difference of input voltage (V_{dc}) and capacitor voltage (V_c). And the load current flows through V_{dc} – capacitor - Load - S_2 and V_{dc}. The output voltage is follows as equation (6).

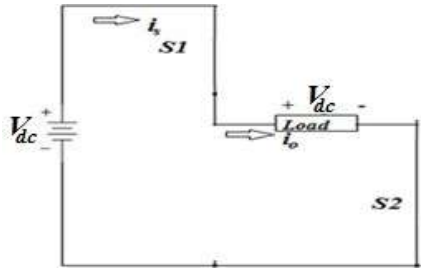


Figure 6(c).Mode3

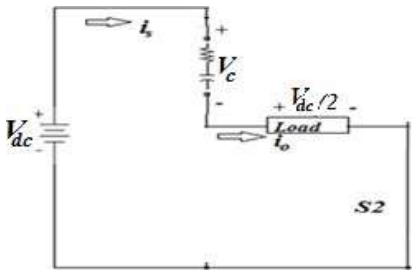


Figure 6(d). Mode4

Mode 5: During this period the switches S_2 and S_4 are closed. The output load voltage is zero i.e. load is short circuited. The output voltage is follows as equation (5)

Mode 6: During this period the switch S_4 is closed. The output load voltage is equals to the difference of input voltage (V_{dc}) and capacitor voltage (V_c). And the load current flows through V_{dc} - capacitor - Load – S_1 and V_{dc}.

$V_o = - (V_{dc} - V_{c)} = -V_{dc}/2$ (8)

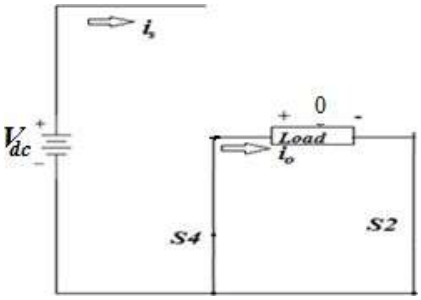


Figure 6(e).Mode5

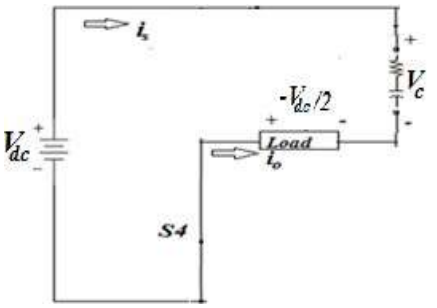


Figure 6(f). Mode6

Mode 7: During this period the switches S_3 and S_4 are closed. The output load voltage is equals to the negative of input voltage (V_{dc}) i.e. load is connected across source directly. And the load current flows through V_{dc} – S_3- Load- S_4andV_{dc}.

$V_o=-V_{dc}$ (9)

Mode 8: During this period de the switch S_2 is closed. The output load voltage is equals to the negative difference of input voltage (V_{dc}) and capacitor voltage (V_c). And the load current flows through V_{dc} – capacitor - Load - S_2 and V_{dc}. The output voltage is follows as equation (8) and this cycle will repeats continuously.

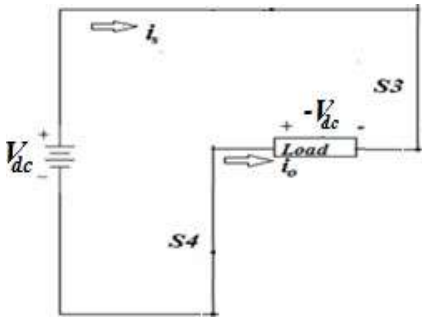


Figure 6(e).Mode7

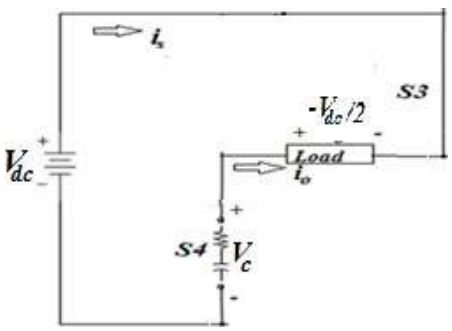


Figure 6(f). Mode 8

The Table 2. Shows the different swiching states of proposed full bridgeinverter.

Table 2. switch states of proposed full bridgeinverter

State	Switches Closed	Vo
1	S1 & S3	0
2	S1	+ $V_{dc}/2$
3	S1 & S2	+ V_{dc}
4	S2	+ $V_{dc}/2$
5	S2 or S4	0
6	S4	- $V_{dc}/2$
7	S3 & S4	- V_{dc}
8	S3	-$V_{dc}/2$

IV. COMPARISON OF PROPOSED STRUCTURE WITH CONVENTIONALSTRUCTURE

The conventional full bridge inverter output voltage or current could be either 0 or $\pm V_{dc}$. These inverters are also named as two level inverter. To get a qualitative voltage waveform and current with reduced amount of ripple content, these inverters require higher frequency of carrier signal along with different pulse-width modulation (PWM) techniques. However in high-power applications, these two level inverters have certain confines like conduction losses and device ratings. Table 3 gives the compaision between conventional two level inverter and the proposed five level (line voltage)inverter.

Table 3. Comparison between conventional and proposed structures

Parameter	Conventional Full bridge inverter	Proposed inverter
No of output voltage levels	2(line voltage)	5(line voltage)
Total harmonic distortion	48%	19.60%
Voltage stresses across switches	high	Low
Output power	low	High
Electromagnetic interference	high	Low
dv/dt ratio	high	Low
Output voltage wave shape	Square wave	Approximate sine wave

The proposed inverter gives a qualitative voltage and current waveform with reduced ripple content. Also this inverter is help full in reactive power compensation. With this proposed structure it may easier to produce a high power, high voltage inverter due to the voltage stresses across each switch is controlled. The limitations of conventional two level inverter are overcome by proposed inverter. Table 4 gives the compaision between three level multilevel inverter and the proposed five level (line voltage) inverter.

Table 4. Comparison between three level multilevel inverter and proposed inverter

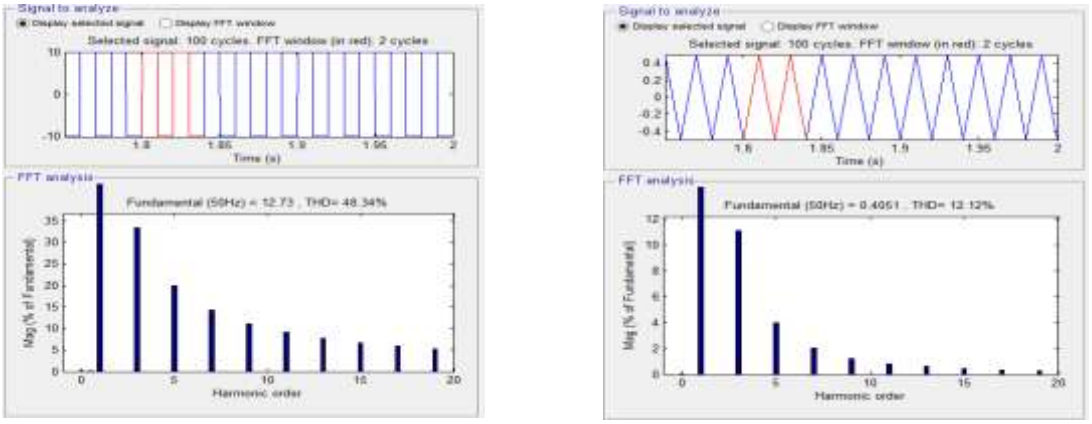
Parameter	Three level multi level inverter	Proposed inverter
No of output voltage levels	5(line voltage)	5(line voltage)
Voltage stresses across switches	medium	Low
No of switches	high	low
Electromagnetic interference	Medium	Low

V. SIMULATION RESULTS

In this section, the MATLAB software is utilized for simulation. Figure 7 shows results of the normal single phase inverter i.e. output voltage output current and their harmonic spectrums. The inverter is having one supply source as DC with a magnitude of 10V. A load which have been taken as the R-L load (R = 1Ω and L = 100mH) for simulation purpose.The switches are IGBT's with internal diodes and having internal resistance of 1m Ω.

The total harmonic distortion (THD) is a popular performance index which estimates the amount of

harmonic content is presented in the output waveform for the power converters. Different modulation methods have been introduced for inverters namely trapezoidal modulation, stepped modulation, SPWM, space vector PWM and modified reference with multi carrierwaveforms.

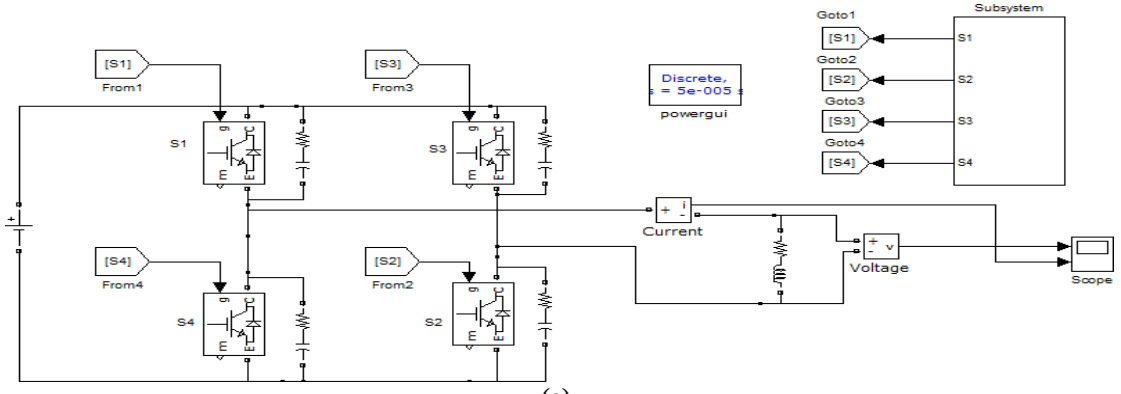


(a) (b)

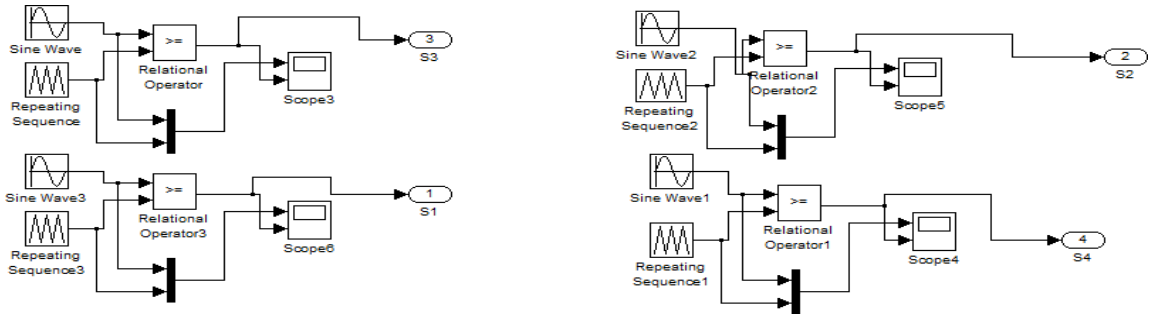
Figure 7. Simulation results for conventional system (a) harmonic spectrum of output voltage (THD=48.34%); (b) Harmonic spectrum of output current (THD= 12.12%)

In this paper, the Sinusoidal PWM has been used. The Sinusoidal PWM technique can eliminate the lower order harmonics along with the control of inverter ouput voltage. The requirement of filter will be minimized as the higher order harmonics can be eliminated easily with SPWM.

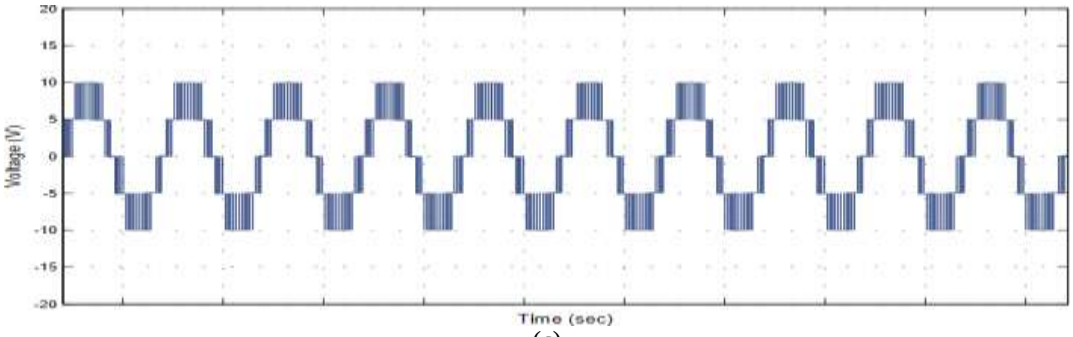
Figure 8 shows the proposed single phase inverter simulation circuit along with its voltage and current waveforms. The inverter is having one supply source as DC with a magnitude of 10V. A load which have been taken as the R-L load (R = 1Ω and L = 100mH) for simulation purpose.The switches are IGBT's with internal diodes and having internal resistance of 1m Ω also having parallel capacitors. Figure 9 shows the harmonic spectrum of output voltage (THD=19.60%), harmonic spectrum of output current (THD= 3.09%) of proposedinverter.



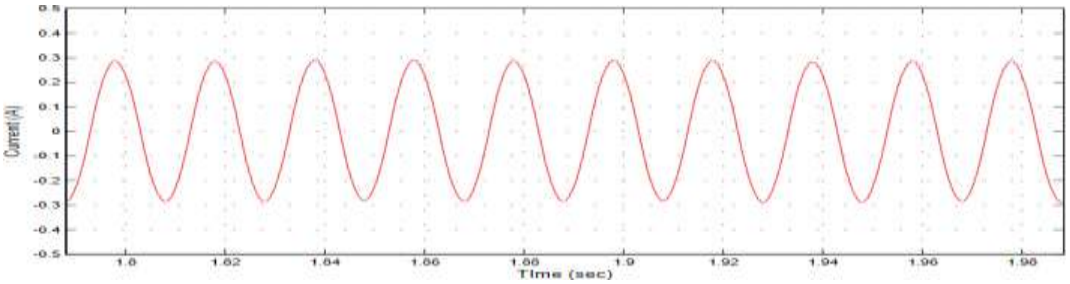
(a)



(b) (b)



(c)



(d)

Figure 8. Simulation results of proposed inverter (a) Circuit diagram; (b) SPWM sequence for switches (sub-circuit); (c) Output voltage; (d) Output current

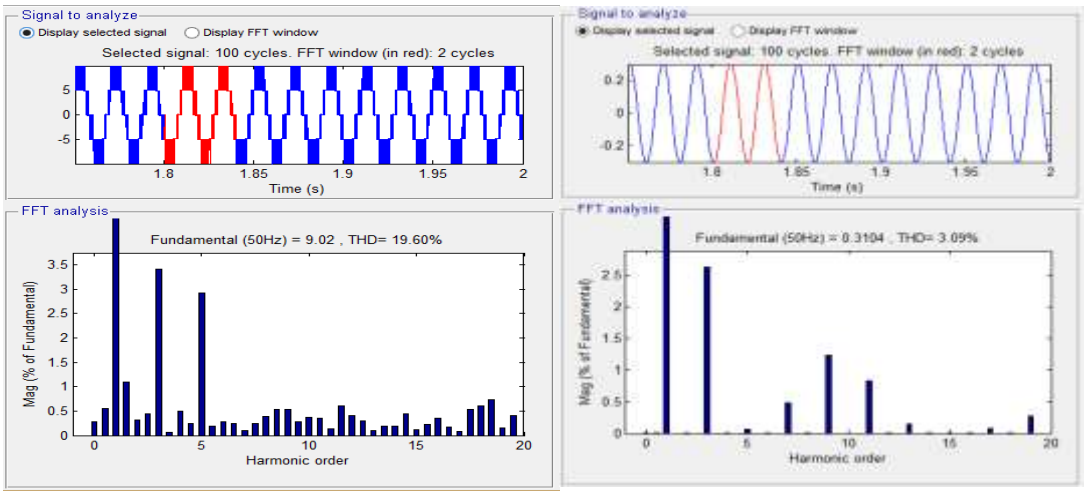


Figure 9. Simulation results for conventional system (a) Simulation output voltage and harmonic spectrum (THD=19.60%); (d) Simulation output current and harmonic spectrum (THD= 3.09%)

VI. CONCLUSION

In this paper, a new multilevel voltage source inverter has been proposed. For the proposed structure, each switch consists of an IGBT and one anti-parallel diode also one capacitor and one resistor are connected across the switch. The proposed inverter gives a qualitative output voltage and current waveform with reduced amount of ripple content. Also this inverter is help full in reactive power compensation. The simulation results have been presented for the proposed inverter using the SPWM technique. From the results of the proposed system THD value is reduced when compare to conventional system. The proposed inverter used in FACTS, UPS, ASDs, and Varcompensators.

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